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(54) **Display apparatus**

(57) Display apparatus comprises a cathode-anode (C—A) matrix of light emitting diodes (LEDs) and for the C lines and for the A lines of the matrix display drivers (5, 6) to sense the voltage level of a respective one of two input signals (VsigC, VsigA) and to switch an electrical current through particular ones of the matrix lines in accordance with the sensed input voltage levels thereby activating a particular LED in the matrix as a visual indication of the relationship between the two input signal voltages. The apparatus is for indicating stereo balance or adjustment in an audio system. The input drivers may include an A—D converter followed by a binary decoder or a priority encoder followed by a binary decoder.

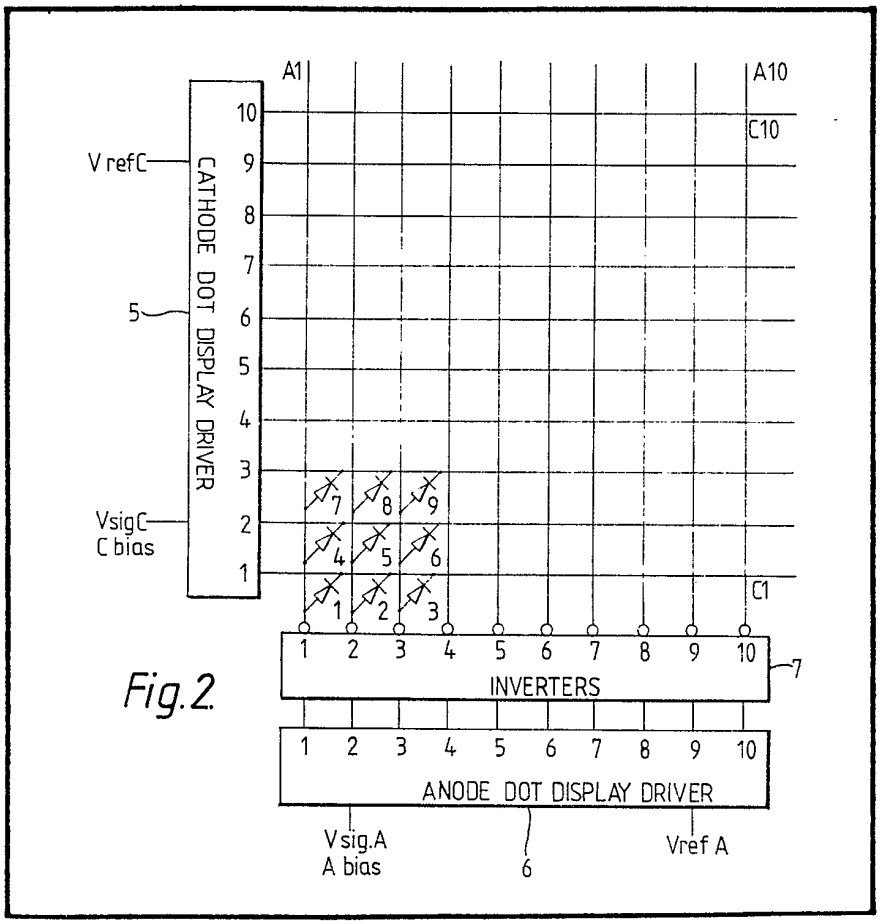

Fig.2.

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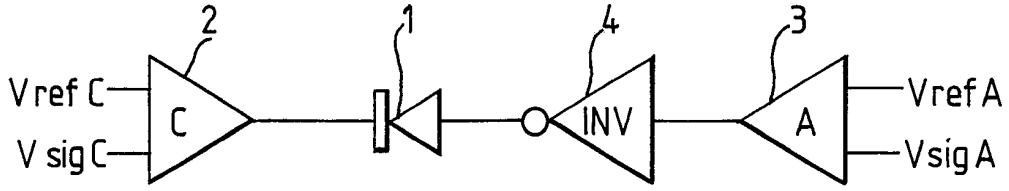

2
1
4
3
Vref C
Vsig C
C
INV
A
Vref A
Vsig A

Fig.1.

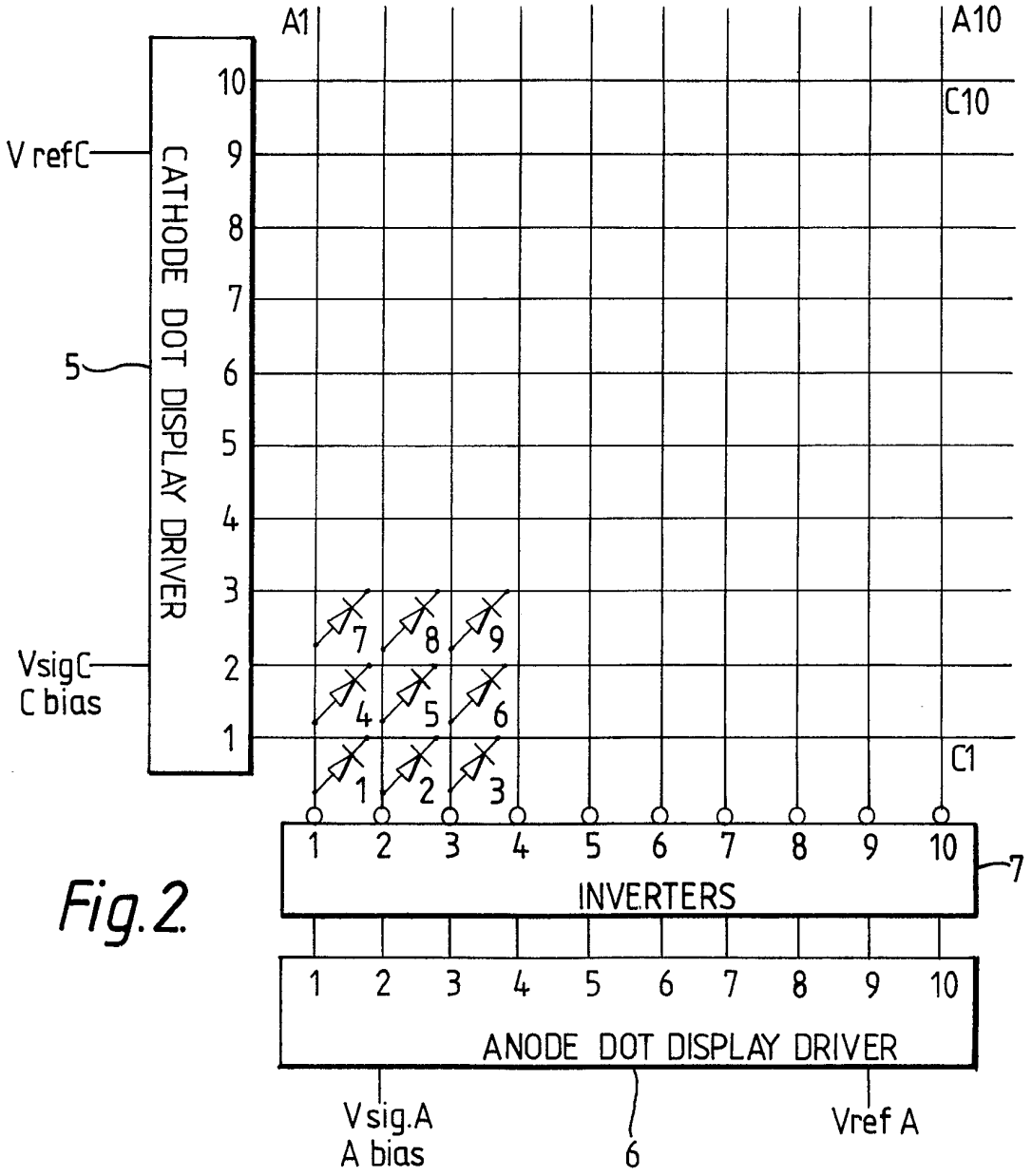

A1
A10
C10
C1
Vref C
5
Vsig C
C bias
CATHODE DOT DISPLAY DRIVER
10
9
8
7
6
5
4
3
2
1
7
8
9
4
5
6
1
2
3
1 2 3 4 5 6 7 8 9 10
INVERTERS
7
1 2 3 4 5 6 7 8 9 10
ANODE DOT DISPLAY DRIVER
Vsig.A
A bias
6
Vref A

Fig.2.

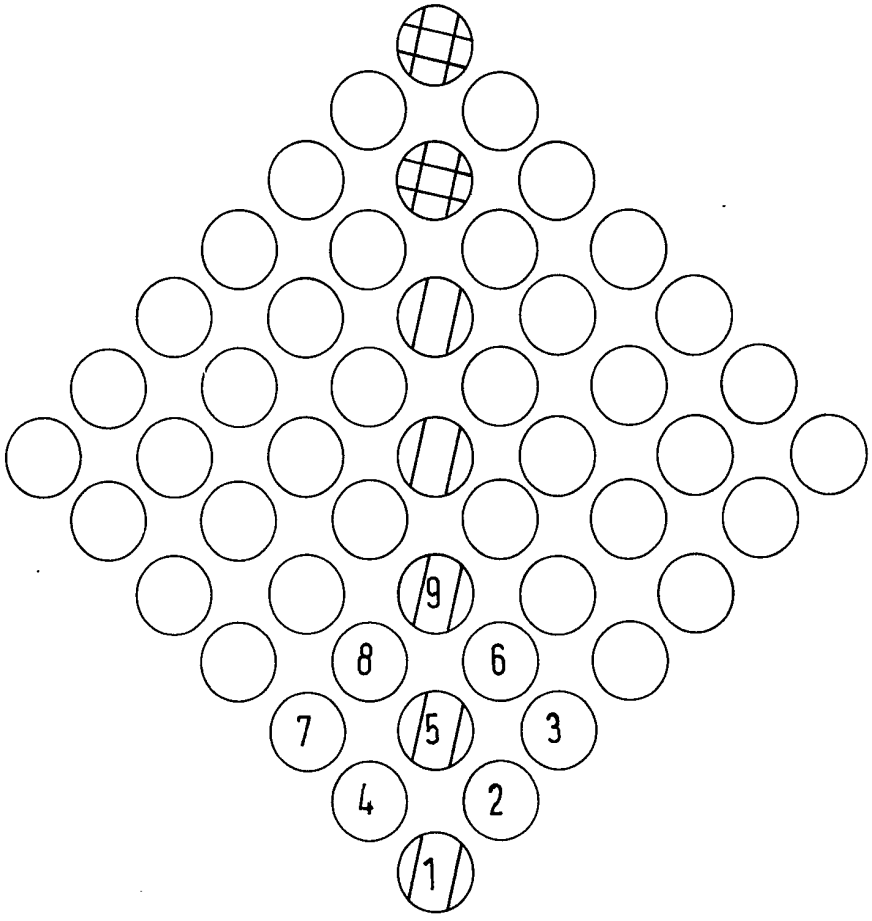


Fig. 3.

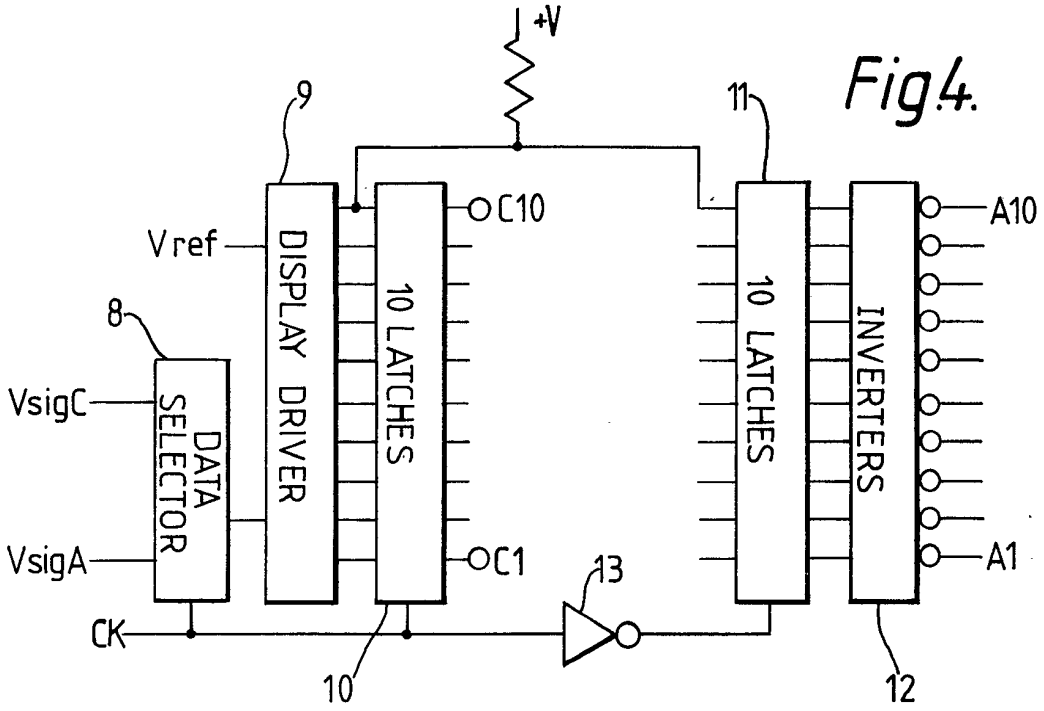

+V
9
11
Vref
8
VsigC
VsigA
CK
DISPLAY DRIVER
DATA SELECTOR
10 LATCHES
10 LATCHES
INVERTERS
C10
C1
A10
A1
13
10
12

Fig.4.

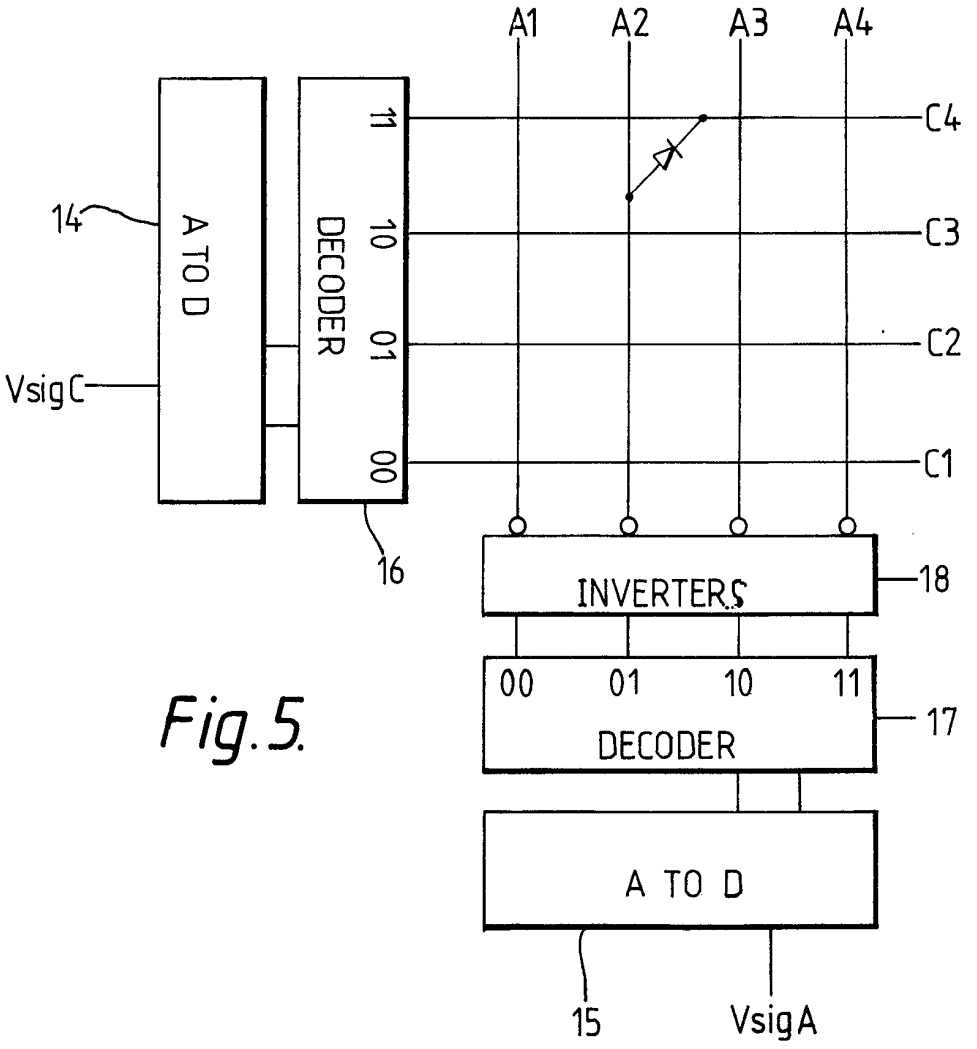
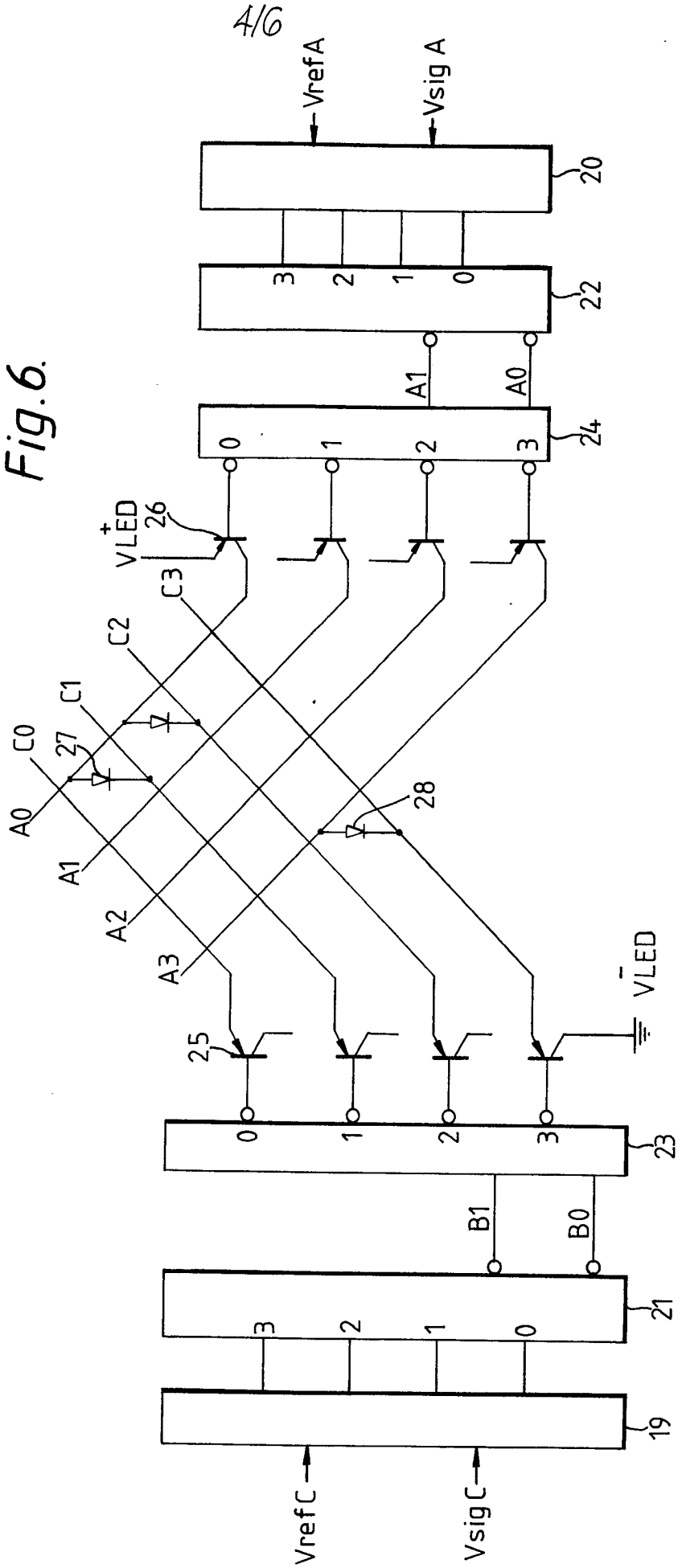

A1
A2
A3
A4
14
VsigC
A TO D
DECODER
11
10
01
00
C4
C3
C2
C1
16
INVERTERS
18
00
01
10
11
DECODER
17
A TO D
15
VsigA

Fig.5.

Fig.6.


VrefA
VsigA
20
22
3
2
1
0
A1
A0
24
0
1
2
3
+
VLED
26
C3
C2
C1
C0
27
A0
A1
A2
A3
28
25
−
VLED
23
0
1
2
3
B1
B0
21
3
2
1
0
19
VrefC
VsigC

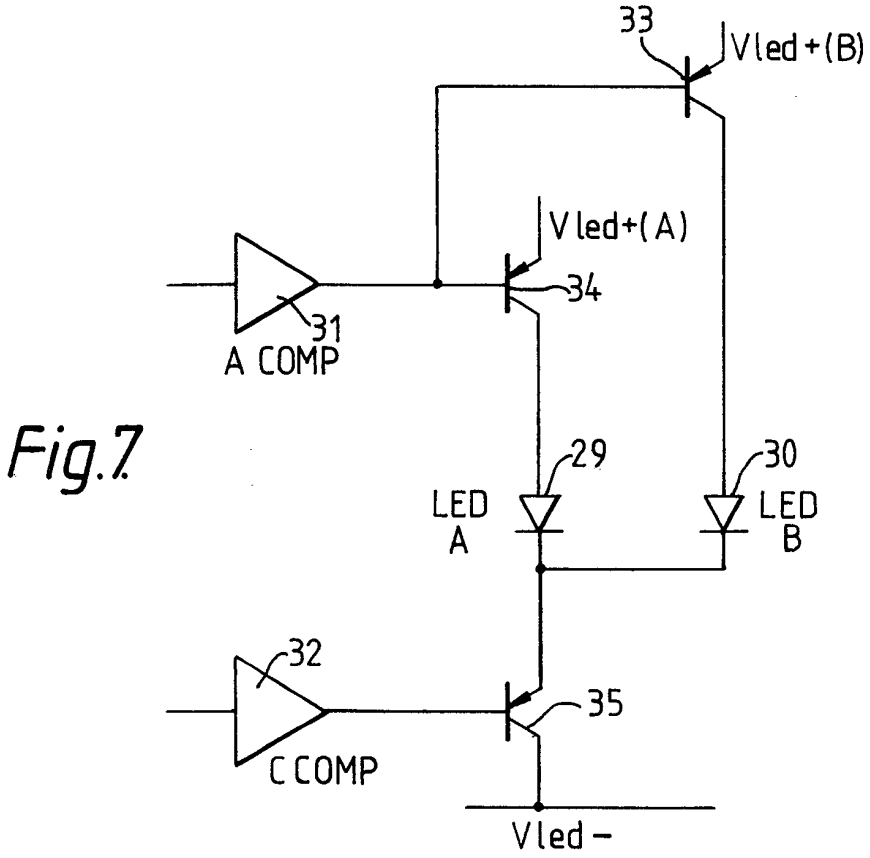

33
Vled+(B)
Vled+(A)
34
31
A COMP
29
30
LED
A
LED
B
32
35
C COMP
Vled-

Fig.7

Fig.8

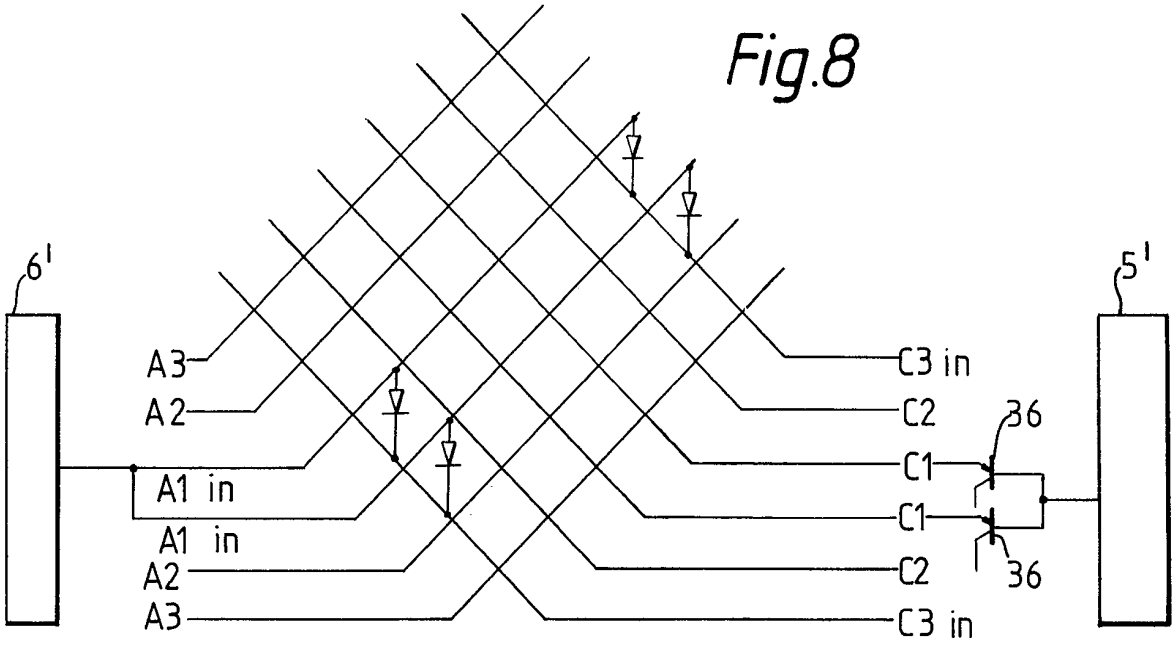
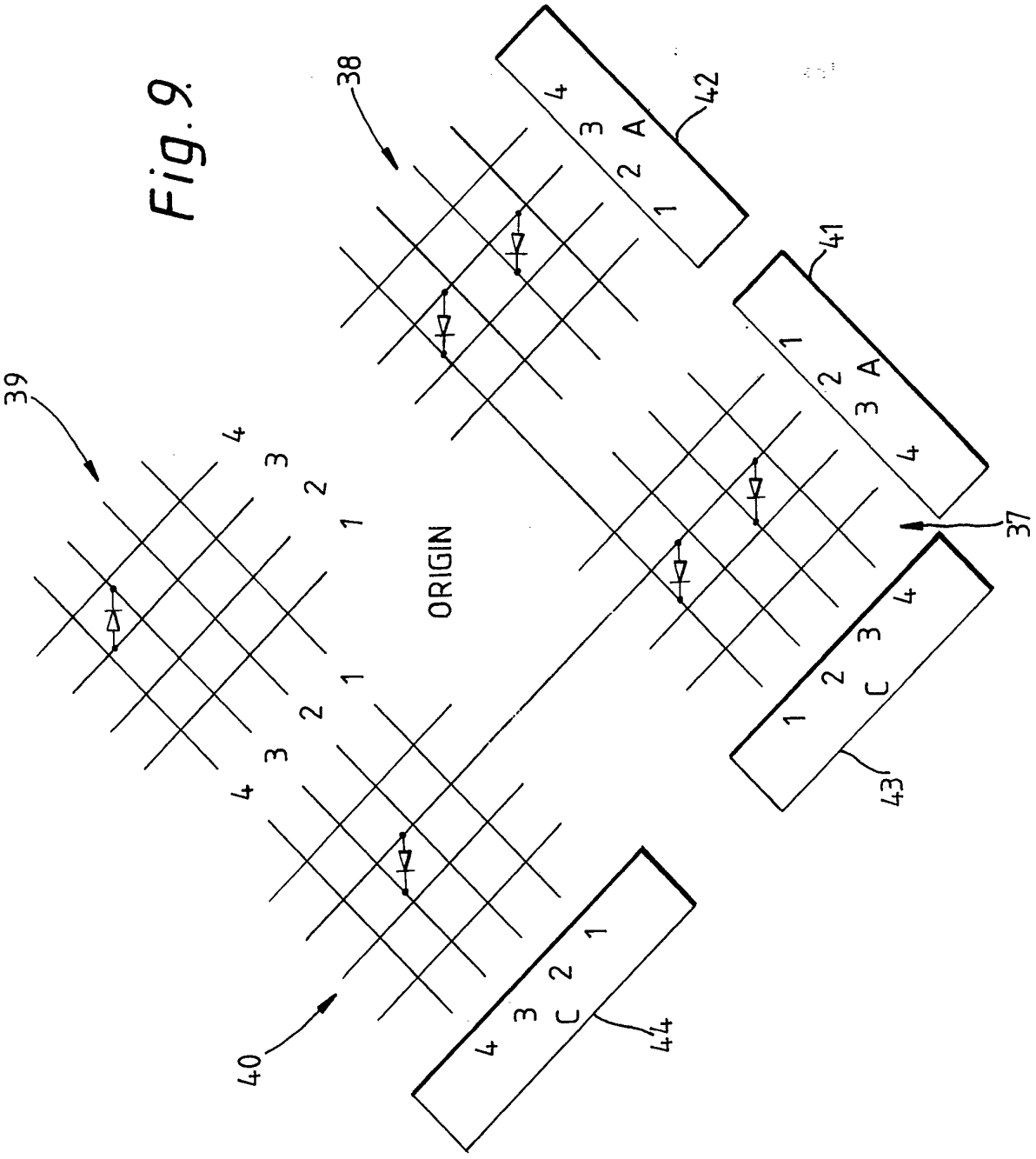

6'
5'
A3
A2
A1 in
A1 in
A2
A3
C3 in
C2
C1
C1
C2
C3 in
36
36

Fig. 9.



SPECIFICATION

Display apparatus

This invention relates to electrical measuring and display apparatus and it particularly, though not exclusively relates to visual display apparatus for indicating stereo balance in an audio system.

There are numerous circuit designs and apparatus known for the detection and visual indication of electrical analogue voltages on an individual signal channel.

One known apparatus is a meter movement with a rectifier and associated electronics. The amount of meter deflection is related to the audio voltage on the channel.

More recent apparatus uses solid state electronic circuits to illuminate a series of visible light emitting diodes (LED's) in either a Bar mode or a moving Dot mode. These displays, sometimes known as "bargraphs" can have different coloured LED's to indicate if signal level is too low, or so high that the level may overload the amplifying chain in the signal channel. The advantage of such apparatus is that, as there are no moving parts, the response to applied audio signals can be much faster than that of a meter indicator, if required.

In a stereo and/or Hi Fi system there is normally one display apparatus connected to give an indication of signal level for each individual channel.

A third display apparatus, which is restricted in use because of the expense and complexity of the circuit arrangement, uses a cathode ray tube (CRT). The signal from one channel is connected to the X deflection circuitry of the CRT and the other channel is connected to the Y deflection circuitry. If there is no signal on either channel the spot will be central on the face of the CRT. A voltage on the X deflection will move the spot horizontally and a voltage on the Y deflection will cause the spot to move vertically. It can be seen that unlike the previous apparatus, a CRT display can not only give an indication of whether the instantaneous signal voltage on any input is positive or negative, but will also show the resultant of the two independent signal inputs. This system can have the fastest response of all and is commonly known as the X-Y mode. It should be noted that input signal paths in an oscilloscope have linear response to give equal increments of spot movement for equal increments of input signal voltage whereas the preferred response and scaling of the indicating means for audio signal measurement is generally of a logarithmic, semi-logarithmic or quasi-logarithmic design and with attack and decay characteristics which further modify the meter response in the presence of rapid signal amplitude variations.

If an identical time varying signal within the audio range of the frequencies is applied to both the X and Y deflection circuitries a straight line at an angle of 45° will appear to be displayed on the CRT. This is caused by (i) persistence of the CRT phosphor, (ii) persistence of vision, and (iii) signal frequency. Any difference in signal level between the two inputs will alter the angle of the line from the horizontal at the extreme of no signal on Y and full amplitude on X to vertical at the other extreme of no signal on X and full amplitude on Y. As the spot position at any instant is determined by the vectorial addition of the two signals the length of the line will vary according to the relative amplitude of the inputs, and be at a maximum when both inputs are of equal value. If the inputs differ in frequency, phase, and/or amplitude the image on the CRT will no longer appear as a straight line, but will give an impression of the overall balance between the signals, or show other harmonic relationships which may be present. It should be noted that by rotating the CRT with its deflection system by 45° in a counterclockwise direction, the image becomes easier to interpret.

In accordance with the present invention there is provided display apparatus comprising a cathode-anode (C-A) matrix of visual elements and for the C lines and for the A lines of the matrix electronic means to sense the voltage level of a respective one of two input signals and to switch an electrical current through particular ones of the matrix lines in accordance with the sensed input voltage levels thereby activating a particular visual element or elements in the matrix as a visual indication of the relationship between the two input signal voltages. This display apparatus provides a means for the visual display of two electrical signals which is simple in construction and economic since it can make use of solid state electronic devices. In most cases, the electronic means will directly sense the voltage levels of incoming analogue signals. However, in some examples, the incoming signals may be in digital form. Furthermore, the electronic means may act on the signals directly or may include storage means for storing, at least temporarily, the incoming signals for later use. This is particularly useful where the visual elements are high power elements which require a finite time to be activated and de-activated.

In one example, the electronic means comprises a C line display driver connected to the C matrix lines; and an A line display driver connected to the A matrix lines, the C and A line display drivers selecting the C and A lines through which electrical current may flow in accordance with the voltage levels of the input signals, the arrangement being such that for each pair of input signal voltage levels current is caused to flow through the selected C and A lines thereby activating one or more visual elements.

Typically, the display drivers referred to above comprise a series of comparators to which an input signal is applied and which compare the input signal with respective different reference voltage levels, the individual reference voltage on each comparator within the display drivers determining the scaling and therefore response of the display to the input signals as linear,

logarithmic, or quasi-logarithmic, the ouptut signal line of the display driver which is activated being determined by the most significant voltage reference level which is equalled or exceeded by the input signal at any instant.

If identical display drivers are used for each signal input, inverting means should be provided between one display driver and the corresponding matrix lines and this may comprise transistors of appropriate type either in the form of discrete devices or as an array in a monolithic package. The display drivers may consist of a series of voltage comparators whose outputs are open collector NPN transistor stages. The uncommitted collector of each output stage operates as a current sink when enabled. Typically, the inversion from current sink to current source is achieved by an appropriate value of pull-up resistor connected between the positive supply line and the comparator output. At the junction between the pull-up resistor and the comparator output, a connection is made to a PNP transistor which will enable as a current source to the respective A line. In a modified form, the inverting means could be TTL or CMOS integrated circuit inverting buffers followed by a power amplifying buffer stage.

In a second example, the electronic means comprises a single display driver, means for connecting the outputs from the display driver alternately to the A lines and the C lines according to which of the two input signals is received; and means for maintaining each connection for the duration of each succeeding connection to enable an electrical current to flow through the selected C and A lines. Conveniently, the means for maintaining each connection comprises registers or latches whose outputs are connected to the corresponding C or A matrix lines either directly or via buffers, power amplifiers and/or inverting means as appropriate.

In a third example, the electronic means comprises a first analogue to digital (A-D) converter for receiving one input signal, the first A-D converter being connected to a first binary decoder whose outputs are connected to one of the A lines and C lines; and a second analogue to digital (A-D) converter for receiving the other input signal, the second A-D converter being connected to a second binary decoder whose outputs are connected to the other of the A lines and C lines, the arrangement being such that for each pair of input signal voltage levels current is caused to flow through a selected A line and C line thereby activating one or more visual elements.

Preferably, a single visual element is activated at each instant in accordance with the voltage levels of the two signal inputs. However, even in this "Dot" mode of operation, the visual appearance of the display gives the subjective impression that a large number of visual elements are simultaneously energised primarily due to persistence of vision and the signal frequency.

In practical electronic circuitry there may be minor transition states where, even in the "Dot" mode of operation, two or more visual elements are simultaneously energised due to switching transients as one output disables and the adjacent output enables. It is a feature of some display drivers operating in "Dot" mode that there is a small overlap between outputs to ensure that at no time will all outputs be disabled other than in the absence of sufficient signal input. Additionaly, the response time of the visual elements themselves can result in two or more such elements being simultaneously in the activated state.

Normally, this overlap in activation is not important but there are occasions when the display apparatus is to be used for accurate measurement purposes when it is desirable to minimise overlap. Preferably therefore the electronic means comprises for the A lines and for the C lines a display driver which receives an input signal; a priority encoder connected to the outputs of the display driver; and a binary decoder connected to the outputs of the priority encoder and whose outputs are connected to the corresponding A lines or C lines, the arrangement being such that for each pair of input signal voltage levels current is caused to flow through a selected A line and C line thereby activating one or more visual elements.

The priority encoder generates a binary output signal corresponding to the highest active (enabled) comparator output from the display driver regardless of whether the lower significant comparator outputs are also enabled as would be the case where the display driver is constructed of discrete comparators, or where the display driver is in monolithic integrated form but operating in "BAR" mode. This binary representation of the analogue input signal is then input to a decoder whose output will enable a particular one of the matrix lines either directly or via an inverter/buffer stage as required. This prevents any possibility of two C or A lines being simultaneously in an activated state and will only allow the visual element or elements of the junction (cross-point) between the selected C line and A line to be activated.

In this latter example, it is particularly convenient if the arrangement is such that when no signal is applied to either of the display drivers, the least significant matrix lines are enabled, causing the least significant visual element to be activated, which would conveniently indicate that the apparatus has power applied. A further advantage of this is that the apparatus can be used to test for the presence and form of a single input signal within the range of measurement of the apparatus, irrespective of whether a second input signal is applied also.

In a further example, at each junction between a C line and an A line there is a group of two or more visual elements.

In some cases, where the incoming signals comprise digital signals, the display drivers are provided by respective ROMs with the input signal being applied along address lines of the ROM and

the matrix lines being connected to the data line outputs of the ROM. In other words, the input digital signal addresses a location in the ROM which address contains data corresponding to one of the matrix lines.

A recent innovation in recording and reproducing sound is the pulse code modulation (PCM) method. With PCM, the temporaly continuous analogue signals on two stereo channels are alternately sampled, the sample value obtained is quantised by an analogue to digital converter to binary symbols and is serially recorded as a bit stream of binary coded pulses. On replay, the alternate left and right serial pulse stream is clocked into a digital to analogue converter, when at the end of each conversion the restored analogue sample value is switched to the appropriate left or right channel.

It should be appreciated that the apparatus of the invention can be utilised to act on PCM signals if the electronic means includes serial in/parallel out shift registers and appropriate latches.

The visual elements preferably comprise light emitting diodes although other electrically energised light sources could be used such as incandescent lamps in which each lamp is wired in series with an insulation diode. Alternatively, liquid crystal phosphorescent or fluorescent displays could be used with appropriate driving electronics. If the power requirements of the visual elements is greater than the electrical output specification of the electronic means such as display drivers and/or inverting means, switching of electric current through the enabled matrix lines and the particular element or elements can be achieved by power amplifying stages, preferably transistors, and/or inverting means which are switched on and off by the instantaneous electrical condition of the output lines from each display driver.

The apparatus is particularly useful where accurate measurements are required for example where a variable frequency within the response limits of the apparatus has to be brought into synchronism with a fixed stable frequency. By applying the two signals to respective inputs and varying the tuning of the variable frequency signal, frequency lock will be indicated by a vertical line of enabled LEDs. If the frequency locks in phase quadrature the display will indicate this condition by enabling a series of LEDs in the shape of an inverted V, corresponding to one quadrant of the Lissajous circle pattern.

Some examples of display apparatus in accordance with the present invention will now be described with reference to the accompanying drawings, in which:—

Figure 1 is a block circuit diagram illustrating how a single visual element can be activated;

Figure 2 is a block circuit diagram of a first example;

Figure 3 illustrates an arrangement of visual elements as presented to a viewer;

Figure 4 is a block circuit diagram of part of a second example;

Figure 5 is a block circuit diagram of a third example;

Figure 6 is a block circuit diagram of a fourth example;

Figure 7 is a circuit diagram of part of a fifth example;

Figure 8 illustrates schematically part of a sixth example; and,

Figure 9 is a schematic block circuit diagram of a seventh example.

In all the examples to be described, the visual elements will be light emitting diodes (LEDs). Figure 1 illustrates the conditions under which an LED 1 may be activated when two independent signal voltage levels VsigC, VsigA, simultaneously equal predetermined and independent reference voltages VrefC, and VrefA. The signal VsigC is applied to a comparator 2 to which is also applied the reference voltage level VrefC while the signal VsigA is applied the reference voltage level VrefA. If both comparators 2, 3 have similar specifications with current sinking output characteristics when enables, i.e. when Vsig=Vref, then an inverter 4 must be positioned in the circuit between the anode of the LED 1 and the output of the comparator 3 so that whenever the output of the comparator 3 is enabled the inverter enables as a current source. Thus at the time when both comparators 2, 3 are enabled, current may flow through the LED 1 causing the LED 1 to illuminate.

If the visual element is a symmetrical device such as a filament lamp it will require a diode of sufficient current handling capacity to be connected in series with it and the inverter 4 will still be required placed at the output of the comparator which connects to the anode side of the series diode.

Figure 2 illustrates the circuit arrangement of a first example. This example has two conventional dot display drivers 5, 6 each having ten output lines. The driver 5, 6 may be National Type LM3914 monolithic integrated circuits which have a linear relationship between the input voltage and the enabled output line, or National Type LM3915 which exhibit a logarithmic relationship to the input. These display drivers 5, 6 have an input buffer which will accept any input voltage within the limits of ± 35 volts which limits can be extended by the addition of appropriate additional circuitry. The input buffer drives 10 individual comparators which are reference to an internal ten step precision voltage divider. A reference voltage VrefC, VrefA determines the turn-on threshold of each comparator, and in dot mode internal circuitry ensures that only one comparator can be enabled at any instant. The ten output lines from the cathode display driver 5 are the C matrix lines of the display, and the ten ouptut lines from the anode display driver 6 are connected to individual inverters 7. The ten outputs from the inverters 7 are connected to the A matrix lines of the display. This 10x10 array of

matrix lines forms a cross-point exchange with LED anodes connected to the A matrix lines and their cathodes to the C matrix lines. For the purpose of illustration only nine LEDs are shown connected (numbered 1 to 9) but it should be understood that a further 91 LEDs could be connected if all cross-points are used. Additionally, it is possible to chain the display drivers and thereby greatly extend the resolution of the display by addition of further LEDs and appropriate adjustment of Vref.

If VrefC and VrefA are the same and VsigC and VsigA are identical audio signals within the response limits of the device and of sufficient amplitude, LED's 1, 5, and 9 will be enabled and disabled in turn in sympathy with the positive excursions of the signals, thus indicating the balanced condition. Persistence of vision will give the impression that these LEDs are continuously lit.

In practice, left and right hand channel signals in a stereo and/or Hi Fi system would have frequency, phase, and/or amplitude differences. If these channel signals were fed to the cathode and anode display drivers 5, 6 respectively and VsigC had three times the amplitude of VsigA, LEDs 1, 4, 7 would illuminate to indicate to the observer the unbalance and enable accurate adjustment of the system to a balanced condition to be made if so desired. If a bias voltage is summed with VsigC and VsigA and this composite signal input to the display drivers 5, 6 the zero signal of the origin of the displayed image can be set to any particular cross-point position. For example, in the absence of signal voltages, the two bias signals can be adjusted until LED 5 is lit and the display will now indicate negative as well as positive excursions of the input signal voltages. In this mode of operation an odd rather than an even number of C and A matrix lines is preferred as such an arrangement will contain one central visual element.

Lissajous figures can be observed, the degree of resolution being determined by the number of cross-points and LEDs in the apparatus.

The LEDs in the display can be of different colours or intensity to assist in assessing signal balance or to indicate excessive signal amplitude, or merely to produce an attractive display. The display may be placed behind a translucent screen, projected through a lens onto a viewing surface, or transmitted by fibre optics to a front panel. This digitised display of analogue signals has the additional advantage of compactness when compared for example with a CRT system.

The input signals VsigC, VsigA can be derived from any source and modified as required before application to the display drivers 5, 6. For example, after rectification time constants could be introduced or alternatively full wave rectification may be carried out prior to application to the display drivers 5, 6 and this will have the effect of brightening the display since the same LEDs will be lit more often in each cycle while it also has the advantage of showing rapidly any asymmetry in the applied signals.

Figure 3 illustrates a typical arrangement of light emitting diodes the diamond shown having a particularly attractive appearance particularly when mounted in a box with a square front face. The nine numbered LEDs in Figure 3 correspond to those numbered in Figure 2 although in this case a seven by seven array is illustrated. Clearly, this diamond shape could be extended as required to accommodate larger numbers of LEDs. Differences in cross-hatching indicate differently coloured LEDs, the different colours being used to indicate balance and overload conditions. It should also be noted that if the seven elements in the vertical diagonal including LEDs 1, 5, and 9 appear to be lit continuously because of persistence of vision it would not only indicate that identical signals were present at the two signal inputs, but because of the spatial relationship between the elements, the line of light is longer than it would be if signals of different amplitudes were input.

A second example is shown in Figure 4. In this example, the two input signals VsigC, VsigA are input to a two line to one line analogue data selector 8. A clock generator (not shown) applies a clock pulse CK which would preferably have a 50% duty cycle to the data selector 8 to switch alternately the two input signals to the output of the data selector. The output of the data selector 8 is permanently connected to the signal input of a display driver 9 similar to the display drivers 5, 6 in Figure 2. A common reference voltage level Vref from any source is also applied to the display driver 9. Each of the ten outputs from the display driver 9 are connected to respective cathode latches 10 and anode latches 11, only one of the latter connections being shown for clarity. When the enable input is high, data at each input is transferred to the respective output lines. When the enable input goes low, the information on the inputs at the transition time is retained on the outputs until the next low to high transition. The outputs from the cathode latches 10 are connected to the C lines of the matrix while the outputs from the anode latches 11 are connected to inverters 12 whose outputs are connected to the A lines of the matrix. The clock signal CK is applied directly to the cathode latches 10 and, via an inverter 13, to the anode latches 11.

For the purpose of explanation it will be assumed that when the clock signal CK is high, input signal VsigC is applied to the display driver 9 by the data selector 8. In this state, the high clock signal allows the latches 10 to transfer the output signals from the display driver 9 to the respective latch outputs. At the transition of the clock signal from high to low the logic state of the display driver outputs at transition time will be retained on the latch 10 output. VsigA will now be selected by the analogue data selector 8 and input to the display driver 9 whose output lines will take up new logic states corresponding to the instantaneous amplitude of VsigA. The outputs

from the display driver 9 will be transferred through the latch 11 replacing previously held data as the inverter 13 causes the latch 11 to be enabled.

Figure 5 illustrates a third example in which the input signals VsigC and VsigR are applied to respective analogue to digital converters 14, 15. Typically the converters 14, 15 contain a resistor network, a comparator, control logic, and output latches. Conversion is performed by a successive approximation technique with the unknown voltage compared to the voltages existing at the resistor tie points using analogue switches. When the appropriate tie point is reached conversion is complete and the latch outputs will contain a binary word corresponding to the unknown voltage. In the drawing, for simplicity, only two such outputs are shown for each analogue to digital converter 14, 15, and these two lines can represent four possible input values as they can only represent the binary values of 00, 01, 10, or 11. These output lines are connected to respective binary decoders 16, 17 each of which has four outputs corresponding to the four possible binary input values. The outputs of the binary decoder 16 are connected directly to the C lines of the matrix while the outputs of the binary decoder 17 are connected via inverters 18 to the A lines of the matrix. Only one LED is shown connected in the drawing, and it will be lit if at the end of the analogue to digital conversions the binary value input to the decoder 16 is 11 and the binary value input to the decoder 17 is 01.

Figure 6 illustrates a fourth example comprising a pair of display drivers 19, 20 similar to the display drivers 5, 6 to which are fed reference voltage levels VrefC, VrefA respectively and input signal levels VsigC, VsigA respectively. The outputs from the display drivers 19, 20 are fed to respective priority encoders 21, 22 (such as Texas Instruments SN74148) where the highest active line generates an appropirate binary output. For simplicity each priority encoder 21, 22 is shown with two output lines and thus can provide a signal corresponding to whichever of its inputs 0, 1, 2, 3 is the highest to be activated. The inverted outputs from the priority encoders 21, 22 are fed to binary decoders 23, 24 which provides an output signal on one of its outputs determined by the value of the binary input signal. The output from the binary decoder 23, 24 is inverted and fed to a respective one of a series of PNP transistors 25 which act as buffer amplifying stages with a greater current sinking capacity than the decoder 23, and to a series of PNP transistors 26 which invert the current sink of enabled decoder outputs to current source for the A matrix lines. Each transistor in the series of transistors 25, 26 is connected between an LED activating voltage and ground via the matrix lines.

For the sake of example, it will be assumed that an input signal VsigC is sufficient to turn on the comparator whose output is linked with the input numbered 2 of the priority encoder 21 but is not sufficient to provide a signal to the input numbered 3. These will cause the priority encoder 21 to output a low signal on its line B1 and a high signal on its line B0. These signals are applied to the binary decoder 23 which will cause a low output from its output 1 causing the corresponding PNP transistor 25 to switch on as a current sink enabling the matrix line C1. Similarly, if VsigA is sufficient to cause a signal to be output to the input numbered 3 of the priority encoder 22 this will cause both signals B0, B1 from the priority encoder 22 to switch low. The binary decoder 24 will thus cause the signal from its output 0 to switch low causing the transistor to switch on as a current source and enabling the matrix line A0. Since the matrix lines A0 and C1 are both enabled current may flow through the LED 27 causing it to illuminate.

It should be noted with the present example that if no signal is applied to either of the display drivers 19, 20 both outputs from each priority encoder 21, 22 will be high causing the output lines of the binary decoders 23, 24 to be low thus enabling matrix lines C3, A3. This will then cause the LED 28 to illuminate with the important consequence that in the absence of any signal on one input there will be an indication of the signal amplitude on the other input. With this circuit arrangement, as only one C and one A matrix line can be enabled at any instant, individual comparators could be used as the display drivers 19, 20.

Figure 7 illustrates a fifth example which represents a modification which could be applied to any of the previous examples. In the previous examples, a single LED has been connected at each junction between C lines and A lines (although only a representative number of these have been illustrated in the drawings for clarity). In Figure 7, two LEDs 29, 30 are positioned at the junction between an A line and a C line. The figure illustrates comparators 31, 32 which will be part of respective display drivers as previously described. The output from the comparator 31 is fed to the base of two PNP transistors 33, 34 while the output from the comparator 32 is fed to the base of a PNP transistor 35. The collector of the transistor 33 is connected to the anode of the LED 30 while the collector of the transistor 34 is connected to the anode of the LED 29. The cathodes of the LEDs 29, 30 are both connected to the emitter of the transistor 35. It will be apparent from Figure 7 that when the outputs from both comparators are enabled, current may flow through the LEDs 29, 30 which will be illuminated.

The two LEDs 29, 30 could have different colours and be in a common encapsulation with a common cathode connection or they could be discrete LEDs of the same or different colours. The control of which LED 29, 30 is activated depends not only on the enabling of comparators 31, 32 but also on the supply voltage levels applied to the emitters of the transistors 33, 34.

One application of this example would be to

filter selectively a narrow band of the audio spectrum. When frequencies within the band are present, the appropriate V_{LED} supply would be enabled and indicate to the viewer that these frequencies were present in the composite signal. Alternatively, using three differently coloured LEDs and splitting the audio band into bass, middle, and treble frequencies and using these outputs to switch the respective V_{LED} a multicoloured display could be obtained.

A particularly attractive display is obtained using the matrix shown schematically in Figure 8. In this example which in its simplest form can be obtained by modifying the example shown in Figure 2, display drivers 5', 6' are provided whose outputs are each connected to a pair of C lines or A lines, the pair being symmetrically arranged relatively to one another. Figure 8 illustrates just one such connection for the least significant output. Since four matrix lines are enabled, four LEDs will be activated and the resulting display has the form of a starburst. To prevent current "hogging" each matrix line has a drive transistor/inverter 36 of which only two are shown in Figure 8 connected to lines C1 for clarity.

Figure 9 illustrates an example in which two sets of apparatus are provided, each set comprising two matrices of visual elements 37, 38, 39, 40. Four sets of display driving means 41, 42, 43, 44 are provided, the driving means 41 being connected to the A lines of matrices 37, 40; the driving means 42 being connected to the A lines of the matrices 38, 39; the driving means 43 being connected to the C lines of matrices 37, 38; and the driving means 44 being connected to the C lines of matrices 39, 40. Each driving means 41, 42, 43, 44 comprises a display driver as previously described and, where necessary, suitable inverting means. Each driving means may be connected separately to the appropriate matrices or alternatively, the C lines and A lines of adjacent A matrices may be connected together as is shown in the case of lines C1 of matrices 37, 38 and A2 of matrices 37, 40, with appropriate steps being taken to deal with 'current hogging'.

Four different input signals are applied to respective ones of the driving means 41—44 and these four signals may for example have been derived from surround systems using four microphones. The apparatus shown in Figure 9 is particularly suitable for controlling balance between the four signals. Furthermore, the apparatus enables the relative amplitudes of the four signals to be easily viewed and adjusted.

It will be appreciated that with the addition of microphones and preamplifiers, all the examples of apparatus described can display ambient sound fields. By recording a stable tone of suitable frequency, and replaying the recording into one input of the apparatus whilst applying the tone to the other input an assessment can be made of the performance of the recording and reproducing system.

Claims

1. Display apparatus comprising a cathode-anode (C-A) matrix of visual elements and for the C lines and for the A lines of the matrix electronic means to sense the voltage level of a respective one of two input signals and to switch an electrical current through particular ones of the matrix lines in accordance with the sensed input voltage levels thereby activating a particular visual element or elements in the matrix as a visual indication of the relationship between the two input signal voltages.

2. Display apparatus according to claim 1, wherein the electronic means comprises a C line display driver connected to the C lines; and an A line display driver connected to the A lines, the C and A line display drivers selecting the C and A lines through which electrical current may flow in accordance with the voltage levels of the input signals, the arrangement being such that for each pair of input signal voltage levels current is caused to flow through the selected C and A lines thereby activating one or more visual elements.

3. Display apparatus according to claim 1, wherein the electronic means comprises a single display driver; means for connecting the outputs from the display driver alternately to the A lines and the C lines according to which of the two input signals is received; and means for maintaining each connection for the duration of the next succeeding connection to enable an electrical current to flow through the selected C and A lines.

4. Display apparatus according to claim 1, wherein the electronic means comprise a first analogue to digital (A-D) converter for receiving one input signal, the first A-D converter being connected to a first binary decoder whose outputs are connected to one of the A lines and C lines; and a second analogue to digital (A-D) converter for receiving the other input signal, the second A-D converter being connected to a second binary decoder whose outputs are connected to the other of the A lines and C lines, the arrangement being such that for each pair of input signal voltage levels current is caused to flow through selected C and A lines thereby activating one or more visual elements.

5. Display apparatus according to claim 1, wherein the electronic means comprise for the A lines and for the C lines a display driver which receives an input signal; a priority encoder connected to the outputs of the display driver; and a binary decoder connected to the outputs of the priority encoder and whose outputs are connected to the corresponding A lines or C lines, the arrangement being such that for each pair of input signal voltage levels current is caused to flow through selected C and A lines thereby activating one or more visual elements.

6. Display apparatus according to claim 5, wherein the arrangement is such that when no signal is applied to either of the display drivers, a visual element is caused to be activated.

7. Display apparatus according to any of the

preceding claims, wherein at each junction between a C line and an A line there is a group of two or more visual elements.

8. Display apparatus according to claim 7, wherein each visual element in the group of visual elements is activated in accordance with the frequency characteristics of the input signals.

9. Display apparatus according to any of the preceding claims, wherein the visual elements have different colours.

10. Display apparatus according to any of the preceding claims, wherein the visual elements are light emitting diodes.

11. Display apparatus according to any of the preceding claims, wherein the electronic means is arranged such that for each pair of input signals two C lines and two A lines are selected, the selected C and A lines each being symmetrically arranged.

12. Display apparatus substantially as herein described with reference to any of the examples shown in Figures 1 to 8 of the accompanying drawings.

13. In combination two sets of display apparatus according to any of the preceding claims, each set comprising two of the apparatus arranged in series with either their A lines or C lines connected together, the other of the A lines and C lines of one set being connected to the corresponding A lines and C lines of the other set; and electronic means assocaited with first and second groups of A lines and with first and second groups of C lines to sense the voltage level of a respective one of four input signals and to switch an electrical current to particular ones of the matrix lines in accordance with the sensed input voltage levels.

14. A combination substantially as herein described with reference to Figure 9 of the accompanying drawings.

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